**Homework #5**

1. Construct a 5-to-32 line decoder with four 3-to-8 line decoder with enable and a 2-to-4 line decoder. Use block diagrams for the components, **label all inputs and outputs.**
2. A combinational circuit is defined by the following three Boolean functions:

F 1 = ( y ′ + x ) z

F 2 = y ′ z ′ + x ′ y + y z ′

F 3 = ( x + y ) z

Design the circuit with a decoder and external gates. Draw the diagram, and label all inputs and outputs. (Hints: turn each function to sum of minterms.)

3. Design an active high BCD-to-decimal decoder using the unused combinations of the BCD code as don’t-care conditions

4. Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams and label all inputs and outputs.

1. Implement a full adder with two 4x1 multiplexers. Draw the truth-table, diagram and label the inputs and outputs.
2. An 8x1 multiplexer has inputs A, B, And C connected to the selection inputs S2, S1, and S0, respectively. The data inputs I0 through I7 are as follows

I1 = I2 = 0, I3 = I7 = 1; I4 = I5 = D’; and I0 = I6 = D;

Determine the Boolean function that the multiplexer implements.

1. Using a case statement, write an HDL behavioral description of an eight-bit arithmetic logic unit (ALU). The circuit has a three-bit select bus (Sel), 8-bit input datapaths (A[7:0] and B[7:0]), an eight-bit output datapath (y[7:0]), and performs the arithmetic and logic operations listed below.

Sel Operation Description

000 y = 8’b0

001 y = A & B Bitwise AND

010 y = A | B Bitwise OR

011 y = A ^ B Bitwise exclusive OR

100 y = ~ A Bitwise complement

101 y = A - B Subtract

110 y = A + B Add (Assume A and B are unsigned)

111 y = 8’hFF